On Test Vector Reordering For Combinational Circuits

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Summary

The cost of testing is a major factor in the cost of digital system design. In order to reduce the test application time, it is required to order the test vectors in such a way that it reduces the time a defective chip spends on a tester until the defect is detected. In this paper, we propose an efficient test vector reordering technique that significantly reduces both the time and memory complexities of reordering procedures based on fault simulation without dropping. Experimental results demonstrate both the efficiency and effectiveness of our proposed technique.

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